

REMARKS

Claims 9, 10, 24, and 26 have been amended. Claims 1-8 and 15-23 were previously withdrawn. Claims 9-14 and 24-26 remain for consideration in the application.

Claim Rejections Under 35 U.S.C. § 103

Claims 9-14 and 24-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over McConnell et al. (U.S. Patent No. 5,986,952). Applicant again traverses this rejection.

McConnell et al. is explicit in its reliance on a redundancy detection device 4 and a repair device 5, and always uses redundancy in its structure. On the other hand, the specification of the present invention, which must be consulted to determine the scope of the claims in the application, explicitly discusses operation without the need for a repair device. The error correction circuitry is built right into the memory device, in an on-chip fashion, therefore eliminating the need for a microprocessor or external hardware to perform detection and correction. No embodiment of McConnell is without the redundancy and external hardware/processor for doing the actual work that is performed on-chip in the present claims. Specifically, claims 9, 10, 24, and 26 have been amended to more clearly state the nature of the error correction used. Since McConnell requires redundancy, and does not provide the on-chip error correction without the use of external decoding hardware/processors, the claims are allowable over McConnell et al.

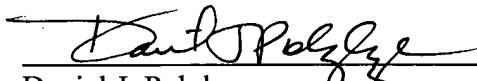
The remaining claims are dependent on and further define one of patentably distinct claims 9, 10, or 24, and are also believed allowable.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2203.

Respectfully submitted,

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